WHAT IS CLAIMED IS:

1. A semiconductor die carrier comprising:

a plurality of electrically insulative side walls;

a plurality of electrically conductive leads extending from at least one of the side walls, each of the leads being individually manufactured without use of a lead frame;

a semiconductor die positioned such that the electrically conductive leads are disposed at one or more locations around the periphery of the die; and

means for providing electrical connection between the semiconductor die and corresponding ones of the electrically conductive leads.

2. A semiconductor die according to claim 1, further comprising an insulative floor, fastened to the side walls, for supporting the semiconductor die, the semiconductor die having a plurality of bonding pads formed thereon.

3. A semiconductor die carrier according to claim 2, the conductive leads comprising a plurality of vertically spaced rows of multiple conductive leads extending from each of the side walls.

4. A semiconductor die carrier according to claim 3, further comprising an insulative ledge, formed between adjacent

ones of the plurality of vertically spaced rows, for supporting the leads.

5. A semiconductor die carrier according to claim 3, the semiconductor die carrier having at least four side walls, and each of the side walls receiving a plurality of the vertically spaced rows of multiple conductive leads.

6. A semiconductor die carrier according to claim 5, wherein each of the side walls receives at least two of the vertically spaced rows of multiple conductive leads.

7. A semiconductor die carrier according to claim 5, wherein each of the side walls receives at least three of the vertically spaced rows of multiple conductive leads.

8. A semiconductor die carrier according to claim 5, wherein each of the side walls receives at least four of the vertically spaced rows of multiple conductive leads.

9. A semiconductor die carrier according to claim 3, wherein each of the leads extends through a corresponding one of the side walls and comprises:

a bonding extension section extending from a position adjacent an inner surface of the side wall in a direction toward the semiconductor die, the bonding extension section including a bonding terminal;

a stabilizing section disposed within the side wall; and

an external lead section extending from a position adjacent an outer surface of the side wall in a direction away from the semiconductor die, the external lead section including a foot section for electrically interfacing with an interface surface.

10. A semiconductor die carrier according to claim 9, the foot section being configured for surface mounting on a PCB.

11. A semiconductor die carrier according to claim 9, the foot section being configured for PTH mounting within a PCB.

12. A semiconductor die carrier according to claim 9, the foot section being configured for pluggable mounting to a PCB or a socket mounted to a PCB.

13. A semiconductor die carrier according to claim 3, wherein, for each side wall, the leads from one of the rows are staggered with respect to the leads from another of the rows.

14. A semiconductor die carrier according to claim 3, wherein, for each side wall, the leads from one of the rows are in a straight alignment with respect to the leads from another of the rows.

15. A semiconductor die carrier according to claim 3, wherein, for each side wall, the leads from one of the rows are staggered with respect to the leads from another of the rows, and the leads from the one of the rows are in a straight alignment with respect to the leads from yet another of the rows.

16. A semiconductor die carrier according to claim 3, the means for providing electrical connection comprising at least one bonding wire connected between one of the bonding pads of the semiconductor die and a bonding terminal formed on one of the leads.

17. A semiconductor die carrier according to claim 3, the semiconductor die being adhered to the floor of the substrate with the bonding pads of the semiconductor die facing up and away from the floor.

18. A semiconductor die carrier according to claim 3, the semiconductor die being adhered to a surface at a position above the leads with the bonding pads of the semiconductor die facing downward.

19. A semiconductor die carrier according to claim 3, the semiconductor die being adhered to the floor within an indentation formed in the floor.

20. A semiconductor die carrier according to claim 3, further comprising a raised platform formed on the floor, the semiconductor die being adhered to the raised platform.

21. A semiconductor die carrier according to claim 3, further comprising an insulative substrate, positioned between adjacent upper and lower rows of the leads and extending beyond the upper row of leads and over the lower row of leads in a direction toward the semiconductor die, for supporting bonding wires connecting the leads to the bonding pads on the semiconductor die.

22. A semiconductor die carrier according to claim 21, further comprising at least one support column supporting the insulating separator.

23. A semiconductor die carrier according to claim 3, wherein the semiconductor die is mounted on a surface suspended above the floor with the bonding pads facing downward toward the floor.

24. A semiconductor die carrier according to claim 3, wherein the semiconductor die carrier has a rectangular shape.

25. A semiconductor die carrier according to claim 3, wherein the semiconductor die carrier has a non-square shape.

26. A semiconductor die carrier according to claim 3, wherein the semiconductor die carrier has at least eight sides.

27. A semiconductor die carrier according to claim 3, wherein each of the side walls comprises at least an inner wall and an outer wall forming a cavity therebetween.

28. A semiconductor die carrier according to claim 27, further comprising bonding material filling the cavity between the inner and outer walls.

29. A method of manufacturing a semiconductor die carrier, the method comprising the steps of:

individually manufacturing a plurality of conductive leads without use of a lead frame;

extending a plurality of the electrically conductive leads from at least one of a plurality of electrically insulative side walls;

positioning a semiconductor die such that the electrically conductive leads are disposed at one or more locations around the periphery of the die; and

electrically connecting the semiconductor die to corresponding ones of the electrically conductive leads.

30. A method of manufacturing a semiconductor die carrier according to claim 29, wherein the step of extending leads from each of a plurality of side walls comprises molding the plurality

of side walls, and inserting each of the leads into one of the side walls.

31. A method of manufacturing a semiconductor die carrier according to claim 29, wherein the step of extending leads from each of a plurality of side walls comprises molding the plurality of side walls around the leads in an insert molding process.

32. A method of manufacturing a semiconductor die carrier according to claim 29, further comprising the step of forming an insulative floor fastened to the side walls for supporting the semiconductor die, the semiconductor die having a plurality of bonding pads formed thereon.

33. A method of manufacturing a semiconductor die carrier according to claim 32, wherein the forming step comprises integrally forming the floor and the plurality of side walls.

34. A method of manufacturing a semiconductor die carrier according to claim 32, wherein the extending step is performed before the floor is fastened to the side walls.

35. A method of manufacturing a semiconductor die carrier according to claim 32, wherein each of the leads is individually inserted into one of the side walls.

36. A method of manufacturing a semiconductor die carrier according to claim 32, wherein the leads are gang-inserted into the side walls.

37. A method of manufacturing a semiconductor die carrier according to claim 32, wherein the leads are formed within the side walls using an insert molding process.

38. A method of manufacturing a semiconductor die carrier according to claim 32, wherein forming of the plurality of side walls comprises, for each side wall, forming at least an outer wall and an inner wall separated by a cavity configured to receive filler material.

39. A method of manufacturing a semiconductor die carrier according to claim 32, wherein each of the leads is inserted into one of the side walls to form a plurality of vertically spaced rows of multiple conductive leads within each of the side walls.

40. A method of manufacturing a semiconductor die carrier according to claim 39, further comprising the step of providing an insulative ledge between adjacent vertically spaced rows to support the leads.

41. A method of manufacturing a semiconductor die carrier according to claim 39, wherein at least two vertically spaced

rows of multiple conductive leads are inserted into each of the side walls.

42. A method of manufacturing a semiconductor die carrier according to claim 39, wherein at least three vertically spaced rows of multiple conductive leads are inserted into each of the side walls.

43. A method of manufacturing a semiconductor die carrier according to claim 39, wherein at least four vertically spaced rows of multiple conductive leads are inserted into each of the side walls.

44. A method of manufacturing a semiconductor die carrier according to claim 39, further comprising the step of positioning an insulating separator between adjacent upper and lower rows of the leads to extend beyond the upper row of leads and over the lower row of leads in a direction toward the semiconductor die to support bonding wires connecting the leads to the bonding pads on the semiconductor die.

45. A method of manufacturing a semiconductor die carrier according to claim 44, further comprising the step of positioning a support column for supporting the insulating separator within the semiconductor die carrier.

46. A method of manufacturing a semiconductor die carrier according to claim 29, further comprising the step, performed after the step of extending leads from each of the side walls, and before the step of positioning the semiconductor die, of carrying out mechanical and/or electrical tests on the semiconductor die carrier.